Advanced

GT24C128H

I2C 128K bits

Serial EEPROM

Table of Contents

1. Features

- Two-Wire Serial Interface, I²C™ Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - Vcc = 1.7V to 3.6V
- Speed: 1 MHZ (1.7V ~ 3.6V)
- Standby current (max.): 1 μA @1.7V
- Read operating current: 1 mA @1.7V
- Write operation current: 2 mA @1.7V
- Sequential & Random Read Features
- Memory organization: 128Kb (16384 x 8)
- Page Size: 64Bytes
- Page write mode
  - Partial page writes allowed
- Self-timed write cycle: 5 ms (max.)
- Configurable Slave address
- Software Write Protection
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- Industrial grade
- Packages: SOIC, TSSOP, UDFN
- Lead-free, RoHS, Halogen free, Green
- Noise immunity on inputs, besides Schmitt trigger

2. General Description

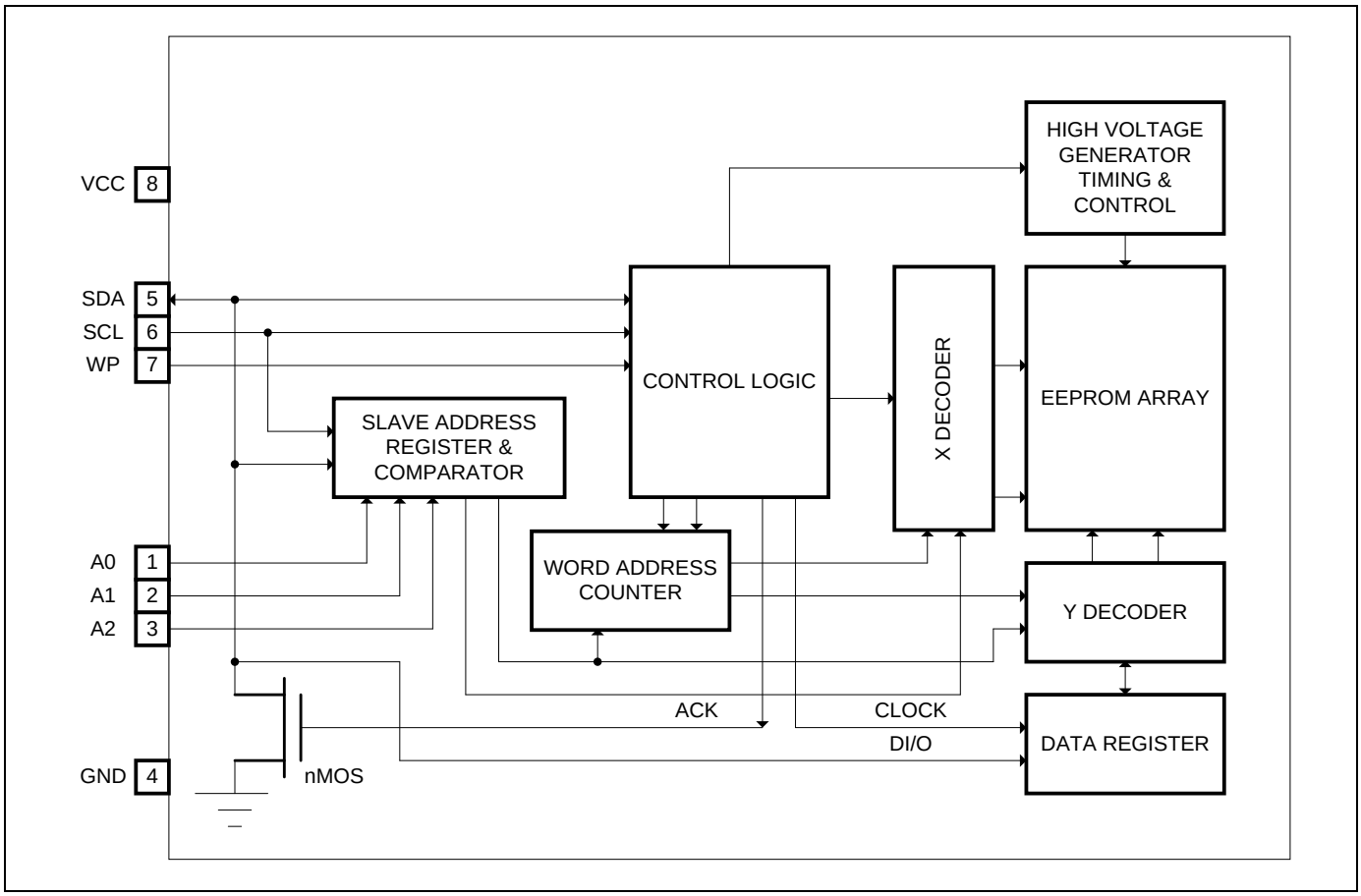
The GT24C128H is an industrial standard electrically erasable programmable read only memory (EEPROM) device that utilizes the industrial standard 2-wire interface for communications. The GT24C128H contains a memory array of 128K bits, which is organized in 64-byte per page.

The EEPROM operates in a wide voltage range from 1.7V to 3.6V, which fits most application. The product provides low-power operations and low standby current. The device is offered in Lead-free, RoHS, halogen free or Green package. The available package type is SOIC, TSSOP, UDFN.

The GT24C128H is compatible to the standard 2-wire bus protocol. The simple bus consists of Serial Clock (SCL) and Serial Data (SDA) signals. Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this GT24C128H. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The device features programmable software write protection and configurable device address.

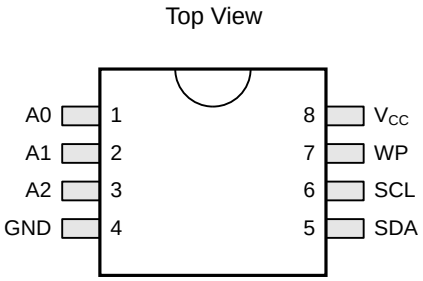
In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the V_{CC} is within its operating level.

3. Functional Block Diagram

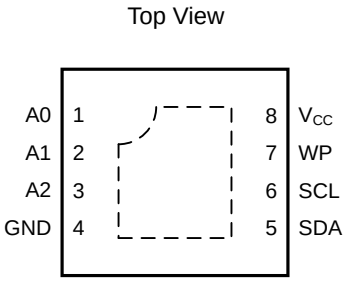


4. Pin Configuration

4.1 8-Pin SOIC, TSSOP



4.2 8-Lead UDFN



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	A0	I	Device Address Input
2	A1	I	Device Address Input
3	A2	I	Device Address Input
4	GND	-	Ground
5	SDA	I/O	Serial Address and Data input and Data out put
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect Input
8	V_{CC}	-	Power Supply

4.4 Pin Descriptions

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain

output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

A0, A1, A2

The A0, A1 and A2 are the device address inputs.

Typically, the A0, A1, and A2 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. When A0, A1, and A2 are left floating, the inputs are defaulted to zero.

WP

WP is the Write Protect pin. While the WP pin is connected to the power supply of GT24C128H, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.

Note: The voltage of WP pin can't rise earlier than Vcc.

V_{CC}

Supply voltage

GND

Ground of supply voltage

Note:

More detail application information, please check application note.

Application note :http://www.giantec-semi.com/Application-note.html

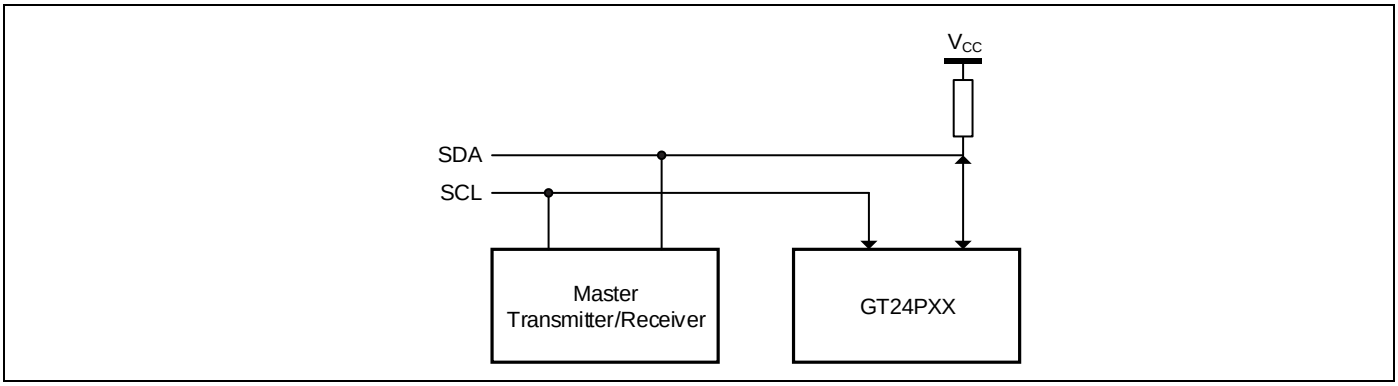
5. Device Operation

The GT24C128H serial interface supports communications using industrial standard 2-wire bus protocol, such as I^2C.

5.1 2-WIRE Bus

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The GT24C128H is the Slave device.

Figure 1. Typical System Bus Configuration

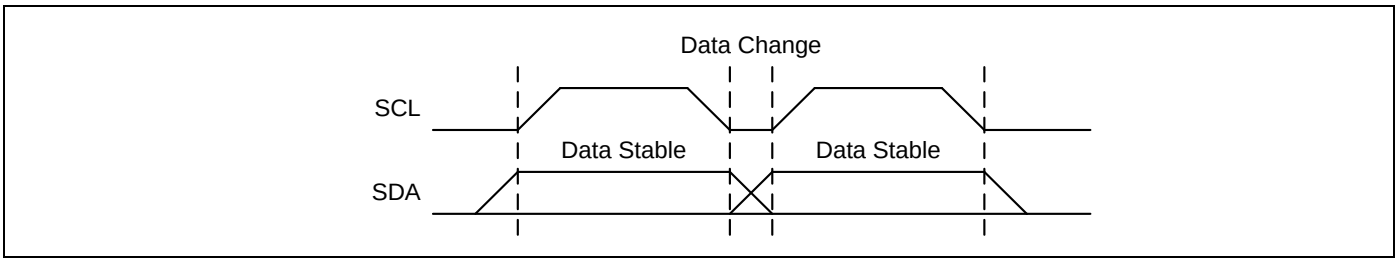


5.2 The Bus Protocol

Data transfer may be initiated only when the bus is not busy. During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

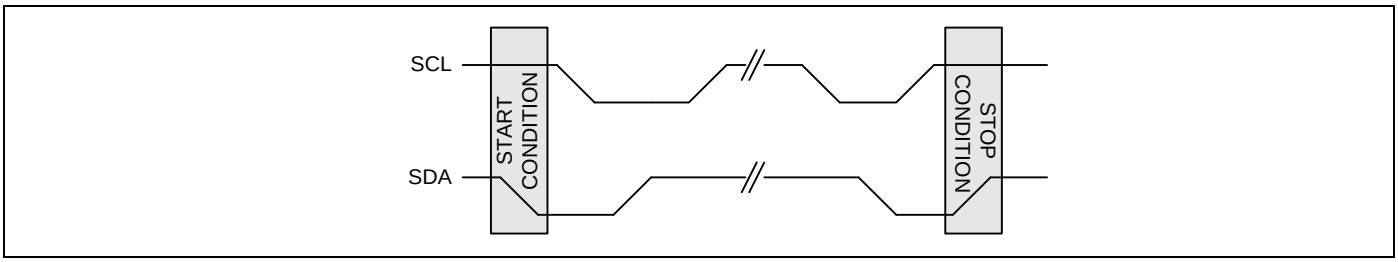
Figure 2. Data Validity Protocol



5.3 Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

Figure 3. Start and Stop Conditions



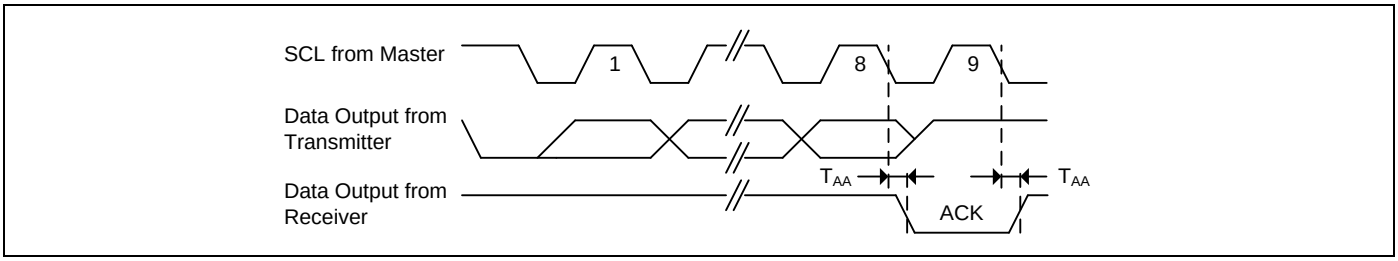
5.4 Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

5.5 Acknowledge

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

Figure 4. Output Acknowledge



5.6 Reset

The GT24C128H contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.) In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

5.7 Standby Mode

While in standby mode, the power consumption is minimal. The GT24C128H enters into standby mode during one of the following conditions: a) After Power-up, while no Op-code is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

5.8 Slave Address

The Master begins a transmission on by sending a Start condition, then sends the address of the particular Slave devices to be communicated.

GT24C128H slave address follows I^2C 7-bit addressing format as shown in Figure 5. The four most significant bits of the Slave address are fixed (1010).the next three bits, A0, A1 and A2, of the Slave address are specifically related to EEPROM as shown in Figure5.

The Device Register is default locked before factory outgoing (Please refer to 6.4)

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

Figure 5. Slave Address

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Slave Address	C6	C5	C4	C3	C2	C1	C0	R/W
Default Value	1	0	1	0	A2	A1	A0	R/W

1. The most significant bit b7 is sent first.
2. Slave Address Code C2 C1 C0 is related to A2 A1 A0 pin

GT24C128H slave address also support 7-bit I^2C addressing format as shown in Figure 6. The most 7 significant bits C6~C0 are configurable via the Device Register after Unlock Device Register by user, then A2,A1,A0 and WP# will be disable. The default setting value of C6:C0 before factory outgoing is 1010 000b.
The Device Register is default locked before factory outgoing (Please refer to 6.4).

Figure 6. Slave Address

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Slave Address	C6	C5	C4	C3	C2	C1	C0	R/W
Default Value	1	0	1	0	0	0	0	R/W

1. The most significant bit b7 is sent first.
2. Slave Address Code C6:C0 is configurable via the Device Register.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, GT24C128H, will respond with ACK on the SDA line. Then GT24C128H will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data. The GT24C128H then prepares for a Read or Write operation by monitoring the bus. The address bytes format is listed in Figure 7, which indicates the master bus which array the master bus would like to access.

Figure 7. Word Address

Note: 'x' indicates don't care

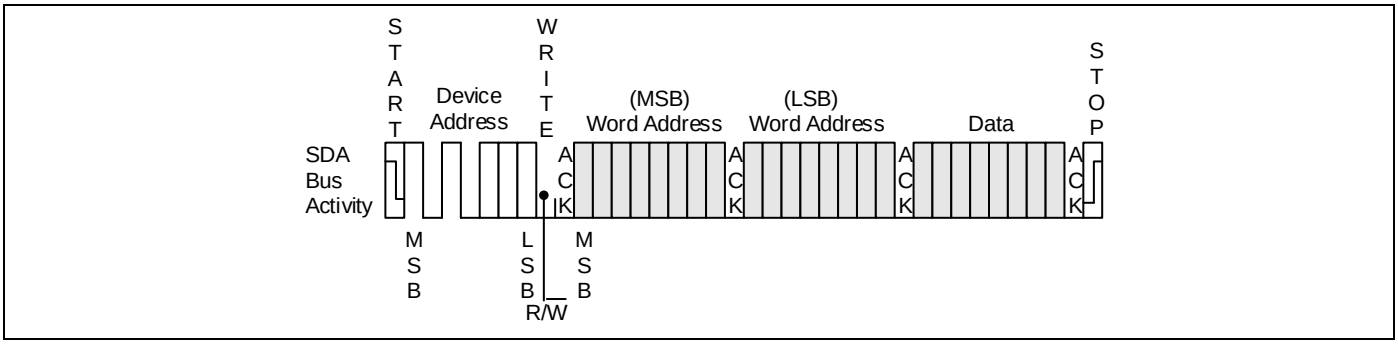
Access Area	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Data memory	0	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Device Register	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x
Lock Device Register	1	0	1	x	x	x	x	x	x	x	x	x	A3	A2	A1	A0
Unlock Device Register	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x
Serial ID	1	0	0	x	x	x	x	x	x	x	x	x	A3	A2	A1	A0

5.9 Write Operation

5.9.1 Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the GT24C128H. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The GT24C128H acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device. (Refer to Figure 8. Byte Write Diagram)

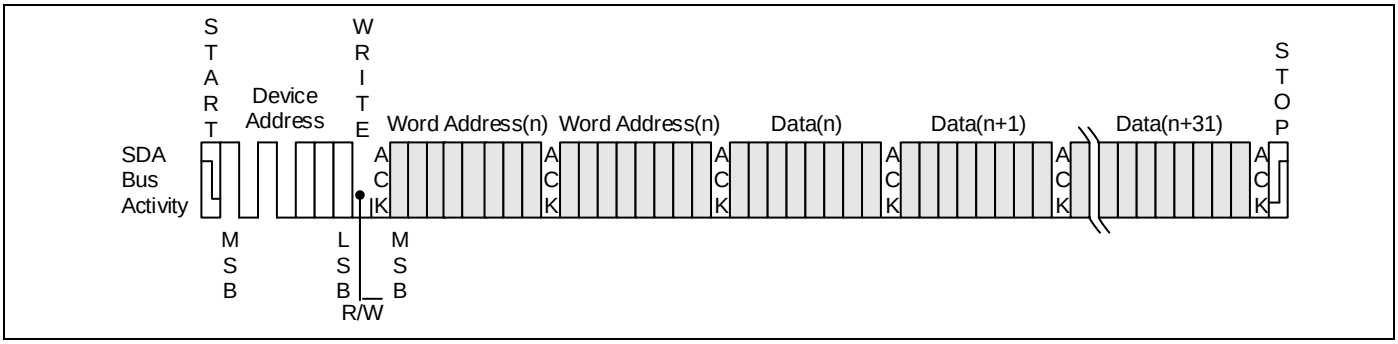
Figure 8. Byte Write



5.9.2 Page Write

The GT24C128H is capable of 64-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 63 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the five lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 64 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 64 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the GT24C128H in a single Write cycle. All inputs are disabled until completion of the internal Write cycle. (Refer to Figure 9. Page Write Diagram)

Figure 9. Page Write



5.9.3 Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the GT24C128H initiates the internal Write cycle. ACK polling can be initiated

immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the GT24C128H has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

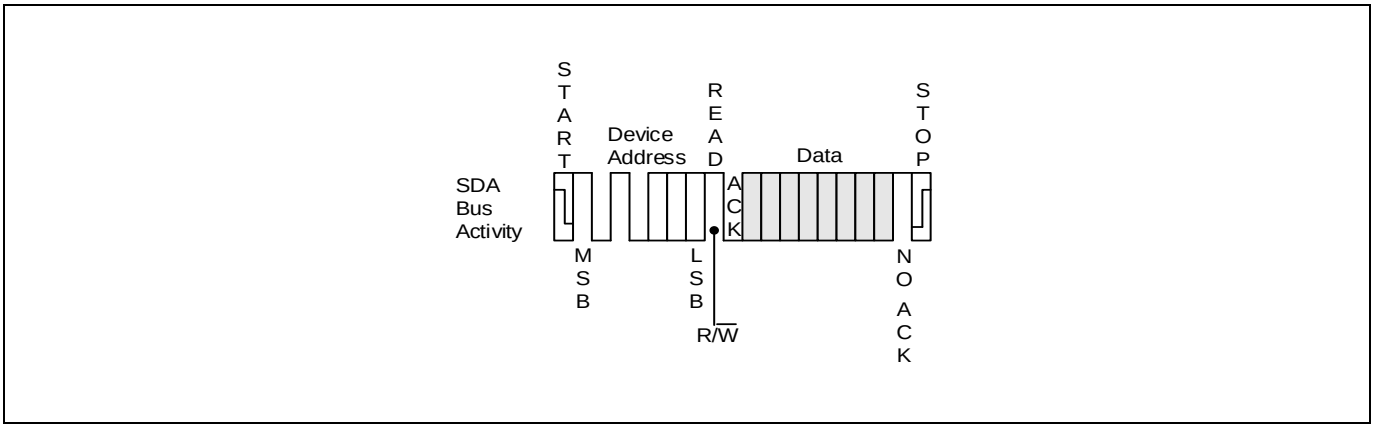
5.10 Read Operation

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read. The default value of read is 0xFF when shipping.

5.10.1 Current Address Read

The GT24C128H contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the GT24C128H discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 10. Current Address Read Diagram.)

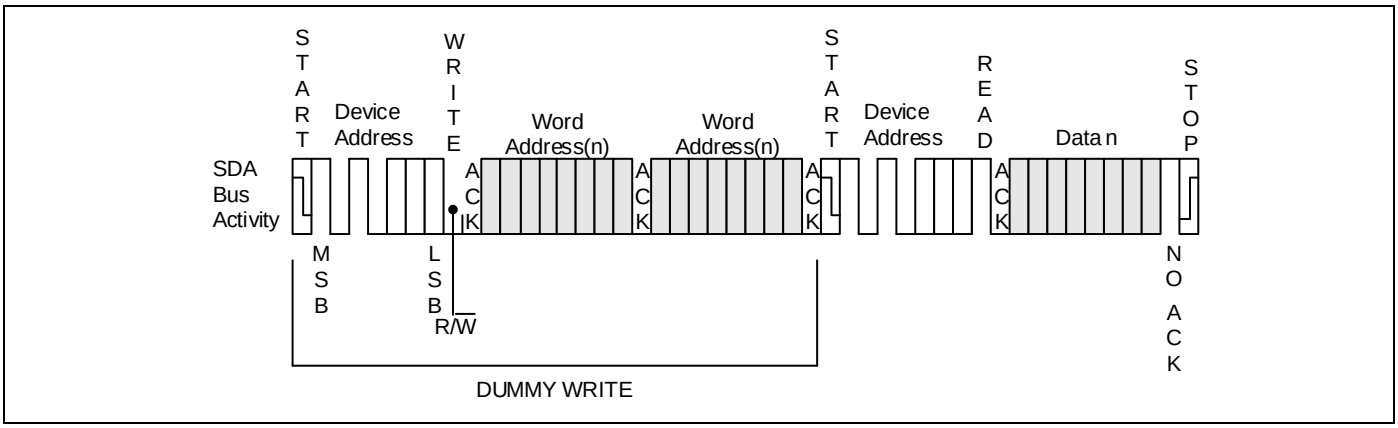
Figure 10. Current Address Read



5.10.2 Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the GT24C128H acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 10. Random Address Read Diagram.)

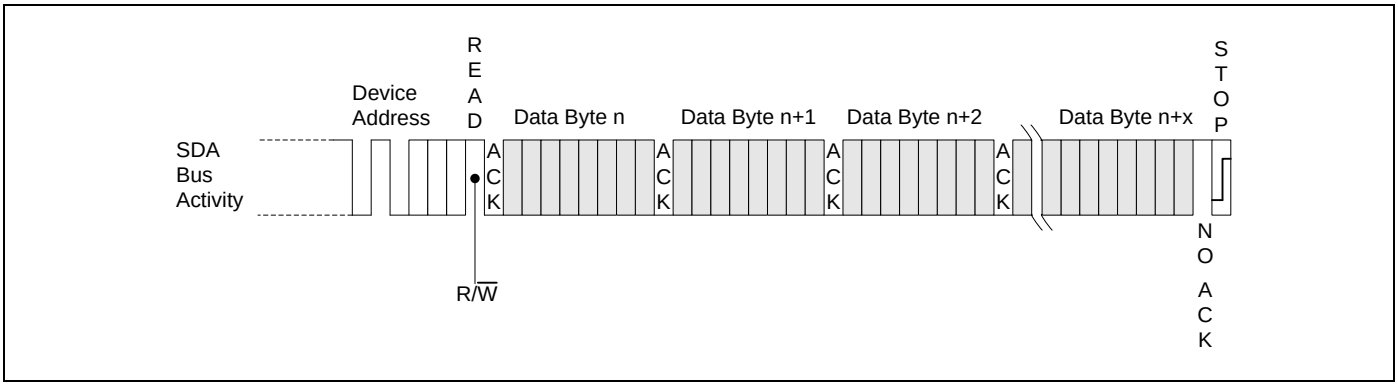
Figure 10 Random Address Read



5.10.3 Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the GT24C128H sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the GT24C128H. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1,n+2 ... etc. The address counter increments by one automatically, allow the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 11. Sequential Read Diagram).

Figure 11. Sequential Read



6. Device Features

6.1 Device Register

This device provides a non-volatile 8-bit register which allows the user to configure the Slave Address and Software Write Protection feature after unlock Device register, then A2,A1,A0 and WP# will be disable, This default value of the register is 1010 0000b,and device register default is Lock(Please check **Lock and Unlock the Device Register** Feature for detail information). Detail description of the Register is shown as below Figure12.

Figure 12. Device Register

Register	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Write	C6	C5	C4	C3	C2	C1	C0	SWP
Read								

Note: 'x' indicates don't care

Bit 7:1 Device address configure bits

The 7 bits are corresponding to C6~C0 bits of the device slave address. The default value is 1010 000b. Totally 128 (2^7) slave address choices can be configured by user. But user must take care the configured slave address must not be conflict with other slave address device on the same master bus.

Bit 0 Software write protection bit

b0 = 0, the whole memory array can be written and read, which is factory outgoing default value.

b1 = 1, the whole memory array is write protected and in read-only mode.

Writing the Device Register:

The first step need to unlock device register, then Writing in the Device Register is performed with a Byte Write instruction at address 111x.xxxx.xxxx.xxxxb (Refer Figure 7 Word Address). Writing more than one byte will discard the write cycle (the Device Register content will not be changed).

If the most significant bits bit7:1 have been re-configured with a correct write command, the device only acknowledge if the salve address is equal to the new values of C6:C0, otherwise No Ack.

Reading the Device Register:

Reading the Device Register is performed with a Random Read instruction at address 111x.xxxx.xxxx.xxxxb (Refer Figure 7 Word Address). Reading more than one byte will loop on reading the Device Register.

6.2 Configurable Device Address

Device Register bits C6:C0 are defining the slave address code in the Slave address. These bits can be written and re-configured with a Write command. Factory delivery value is 1010 000b.

At power up or after reprogramming, the device will load the last configuration value of C6:C0.

6.3 Software Write Protect

In order to prevent unexpected write sequence, this device offers the SWP feature, which makes it possible to protect the whole memory content. Write operations are disabled (read-only memory) when the SWP is set to 1 (SWP=1b). In the same way, the write operations are enabled when the SWP is set to 0 (SWP=0b). Factory default values is 0b.

At power up or after reprogramming, the device will load the last configuration of the SWP value.

6.4 Lock and Unlock the Device Register

The Lock Device Register instruction locks the Device Register in Read-only mode,the lock Device register instruction have two method. This instruction is similar to Byte Write (into memory array) with the following specific conditions:

The Device Register is default locked before factory with Address bit A15:A0 :101X XXXX XXXX 1010b.

- Device type identifier should be aligned to the current setting of Deice Register whose initial setting is 1010 000b.
- Address bit A15:A0 :101X XXXX XXXX 1000b
  Device register can be lock, A2,A1,A0 and WP# is disable, the soft slave address and SWP is active and reading only
- Address bit A15:A0 :101X XXXX XXXX 1010b;
  Device register can be reset to 1010 0000b, and A2,A1,A0 and WP# is active , the soft slave address and SWP is disable
- The data byte must be 0xFF

The locked/unlocked status of the Device Register can be checked by the Lock Device Register instruction.

The device returns an acknowledge bit if the Device Register is unlocked, otherwise a NoAck bit if the Device Register is locked.

The Unlock Device Register instruction unlocks the Device Register in write mode, then A2,A1,A0 and WP# is disable. This instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier should be aligned to the current setting of Device Register whose initial setting is 1010 000b.
- Address bit A15:A13 must be ‘110’; all other address bits are don't care.
- The data byte must be 0x00

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

6.5 Serial ID

The Serial ID is only 16-byte and is Ready-only.

Reading the Serial ID is similar to the sequential read sequence but require use of the device address and dedicated word address (Figure 7). The word address A3~A0 defines the byte address inside the Serial ID. However, it is recommend to set A3~A0 as 0 and the read data bytes must be 16 to guarantee the entire 128-bit value correctly readout.

When the end of 128-bit Serial ID is reached (16-Byte), the data word address will roll-back to the beginning to the 128-bit Serial ID. The Serial ID read operation is terminated when the master does not respond with a zero (ACK) and instead issues a STOP bit.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to V_{CC} + 1	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 1	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40°C to +85°C	1.7V to 3.6V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

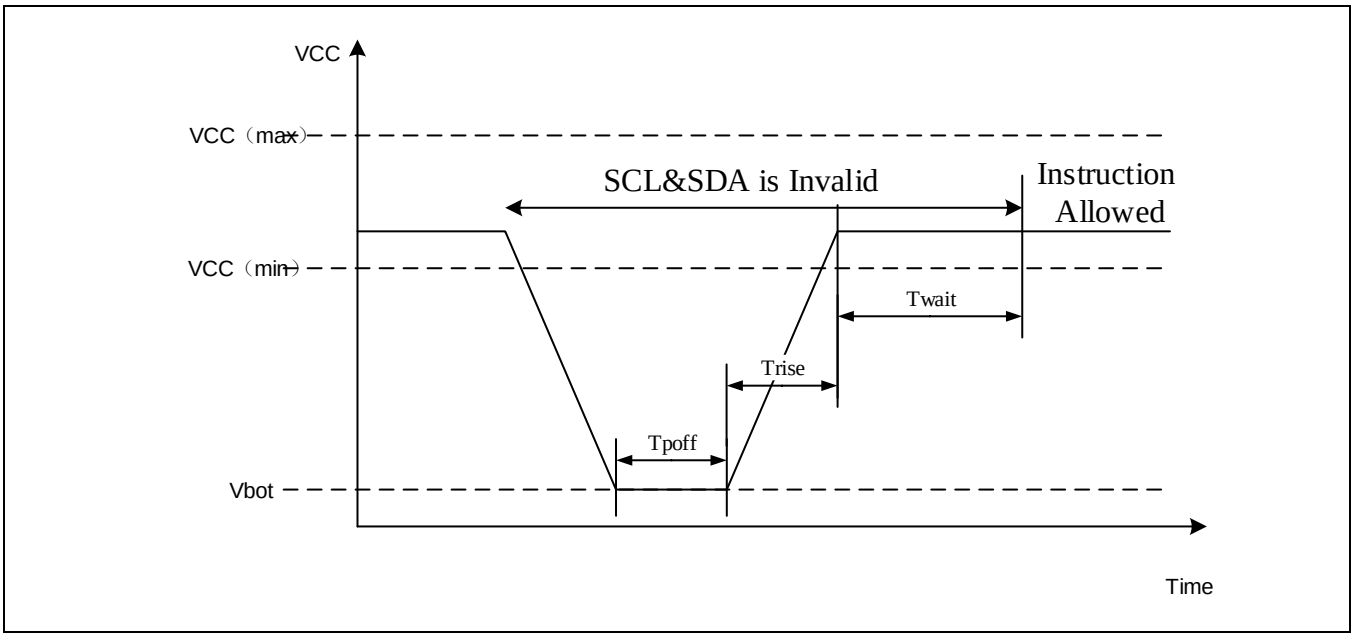
7.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.6V.

7.4 Power Up/Down and Voltage Drop



Power down-up Timing

Symbol	Parameter	min	max	unit
V_{bot}	VCC at power off		0.2	V
Tpoff	VCC at power off time	100		ms
Trise	Vbot to VCC min	0.1	300	ms
Twait	VCC Min to Instruction	2		ms

* All parameters may be changed after the design or process change.

7.5 DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, V_{CC} = 1.7V ~ 3.6V

Symbol	Parameter [1]	Vcc	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			1.7		3.6	V
V_{IH}	Input High Voltage			0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input Low Voltage			-0.5		0.3* V_{CC}	V
I_{LI}	Input Leakage Current	3.6V	V_{IN} = V_{CC} max	—		2	μA
I_{LO}	Output Leakage Current	3.6V		—		2	μA
V_{OL1}	Output Low Voltage	1.7V	I_{OL} = 0.15 mA	—		0.2	V
V_{OL2}	Output Low Voltage	2.5V	I_{OL} = 2.1 mA	—		0.4	V
I_{SB1}	Standby Current	1.7V	V_{IN} = V_{CC} or GND	—	0.2	1	μA
I_{SB2}	Standby Current	2.5V	V_{IN} = V_{CC} or GND	—	0.3	1	μA
I_{SB3}	Standby Current	3.6V	V_{IN} = V_{CC} or GND	—	0.5	1	μA
I_{CC1}	Read Current	1.7V	Read at 1 MHz	—	0.3	1	mA
		3.6V	Read at 1 MHz	—	0.5	2	mA
I_{CC2}	Write Current	1.7V	Write at 1 MHz	—	0.5	2	mA
		3.6V	Write at 1 MHz	—	0.5	3	mA

Note: The parameters are characterized but not 100% tested.

7.6 AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 1.7V to 3.6V

Symbol	Parameter [1] [2]	1.7V≤V_{CC}≤3.6V Slow Mode		1.7V≤V_{CC}≤3.6V Fast Mode		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCK Clock Frequency		400		1000	KHz
T_{LOW}	Clock Low Period	1200	—	400	—	ns
T_{HIGH}	Clock High Period	600	—	260	—	ns
T_R	Rise Time (SCL and SDA)	—	300	—	300	ns
T_F	Fall Time (SCL and SDA)	—	300	—	100	ns
$T_{SU:STA}$	Start Condition Setup Time	500	—	200	—	ns
$T_{SU:STO}$	Stop Condition Setup Time	500	—	200	—	ns
$T_{HD:STA}$	Start Condition Hold Time	500	—	200	—	ns
$T_{SU:DAT}$	Data In Setup Time	100	—	40	—	ns
$T_{HD:DAT}$	Data In Hold Time	0	—	0	—	ns
T_{AA}	Clock to Output Access time (SCL Low to SDA Data Out Valid)	100	900	50	400	ns
T_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	ns
T_{WR}	Write Cycle Time	—	5	—	5	ms
T_{BUF}	Bus Free Time Before New Transmission	1000	—	400	—	ns
T	Noise Suppression Time	—	50	—	50	ns
Endr	Endurance (3.6V, 25C, page mode)	1 million				cycles

Notes: [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 3.6V), 10 kΩ (1.7V)

C_L = 100 pF

Input pulse voltages: 0.3*V_{CC} to 0.7*V_{CC}

Input rise and fall times: ≤ 50 ns

Timing reference voltages: half V_{CC} level

7.7 Timing Diagrams

Figure 13. Bus Timing

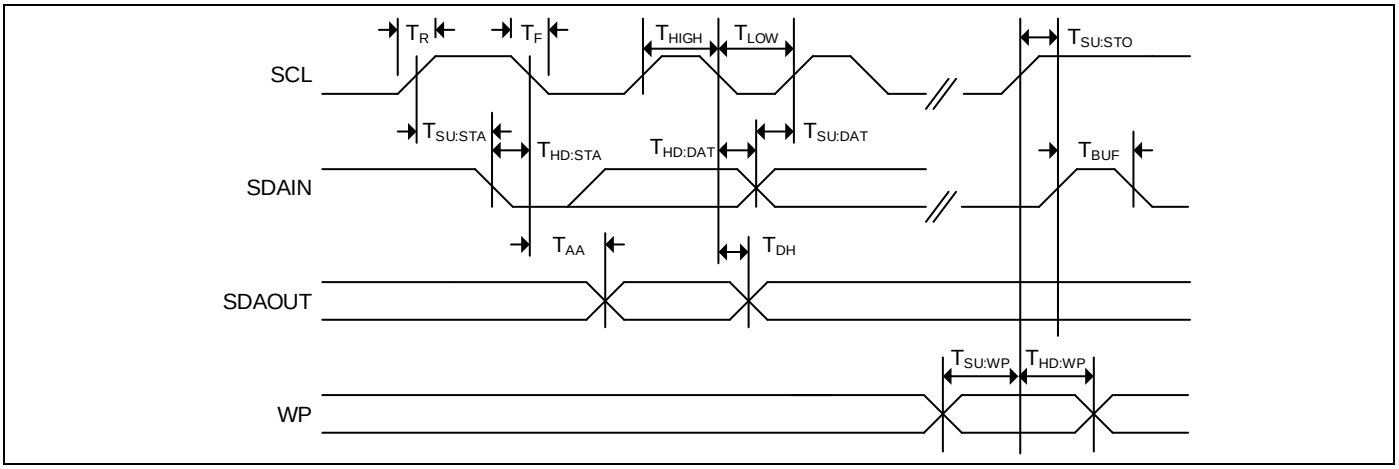
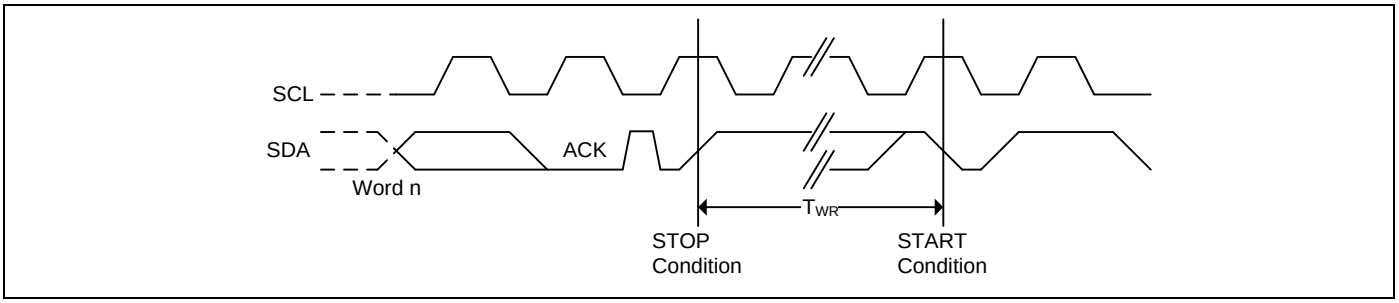


Figure 14. Write Cycle Timing



8. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

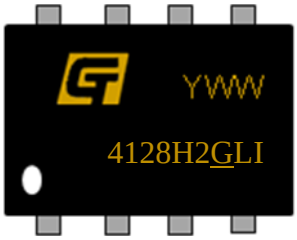
Voltage Range	Part Number*	Package (8-pin)*
1.7V to 3.6V Normal Package	GT24C128H -2GLI-TR	150-mil SOIC
	GT24C128H -2ZLI-TR	3 x 4.4 mm TSSOP
	GT24C128H -2UDLI-TR	2 x 3 x 0.55 mm UDFN

Note:

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel “-TR” (4K per reel).
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.

9. Top Markings

9.1 SOIC package



G: Giantec Logo

4128H2GLI: GT24C128H-2GLI-TR

YWW: Date Code, Y=year, WW=week

9.2 TSSOP package

GT: Giantec Logo

4128H2ZLI: GT24C128H-2ZLI-TR

YWW: Date Code, Y=year, WW=week

9.3 UDFN package

GT: Giantec Logo

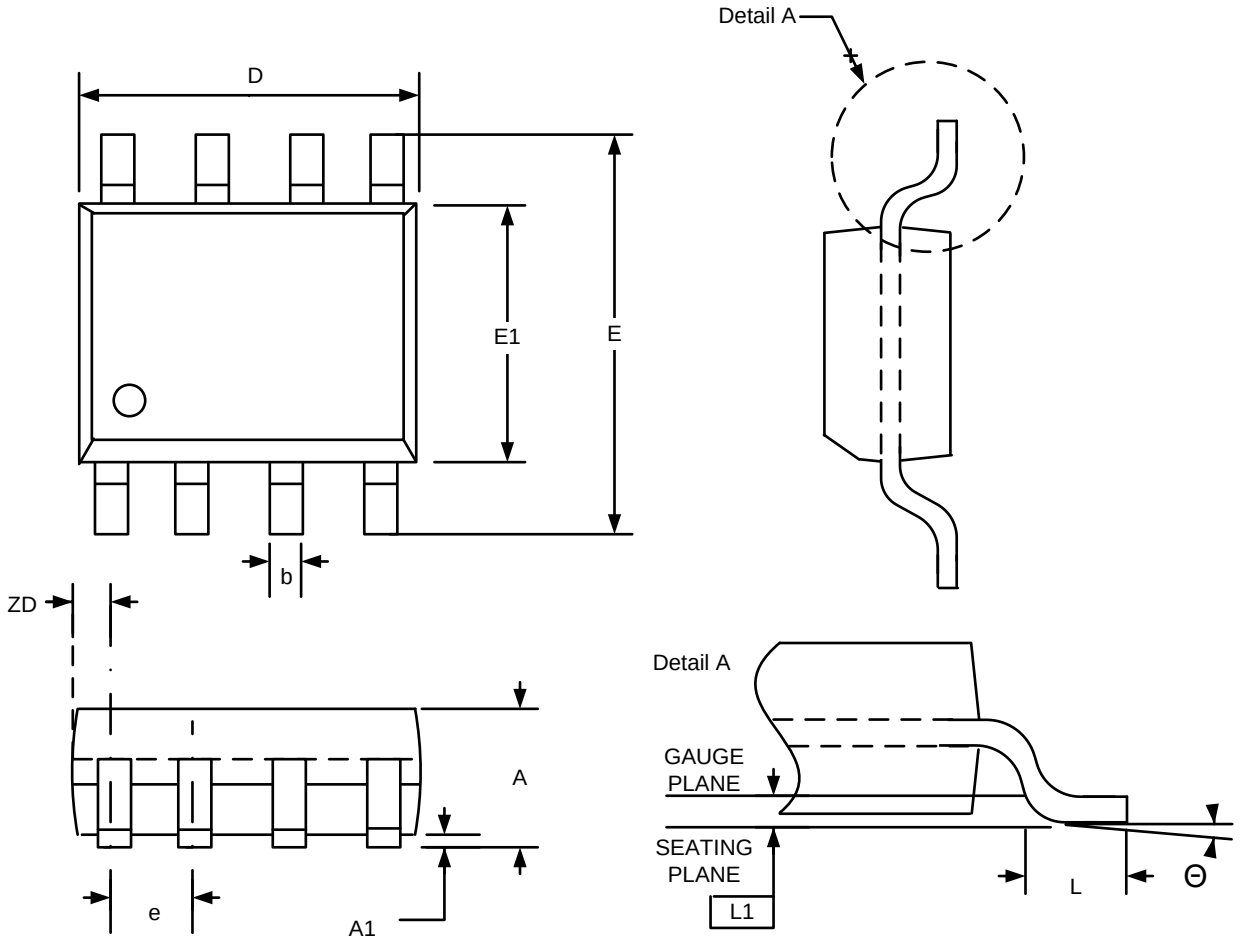
47H: GT24C128H-2UDLI-TR

YWW: Date Code, Y=year, WW=week

10. Package Information

10.1 SOIC

8L 150mil SOIC Package Outline



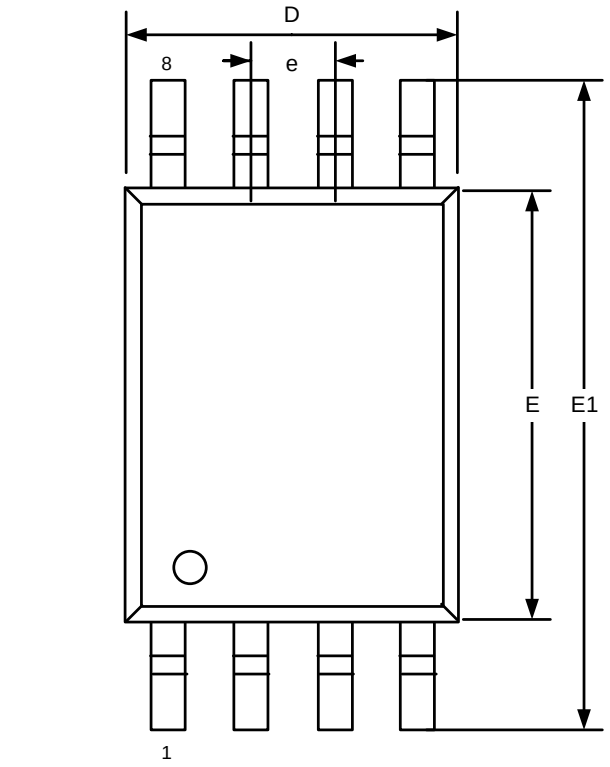
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

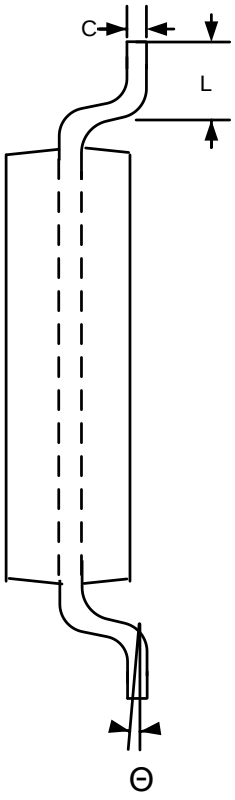
Note:

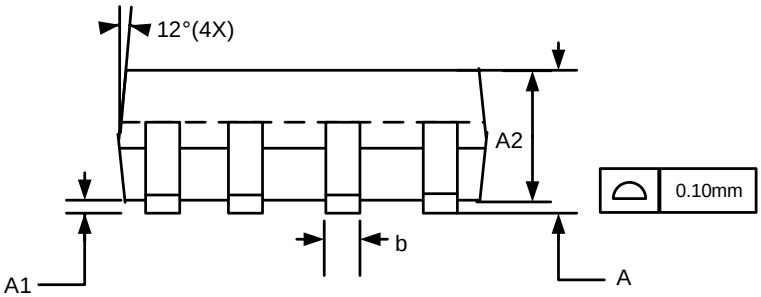
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

10.2 TSSOP

8L 3x4.4mm TSSOP Package Outline





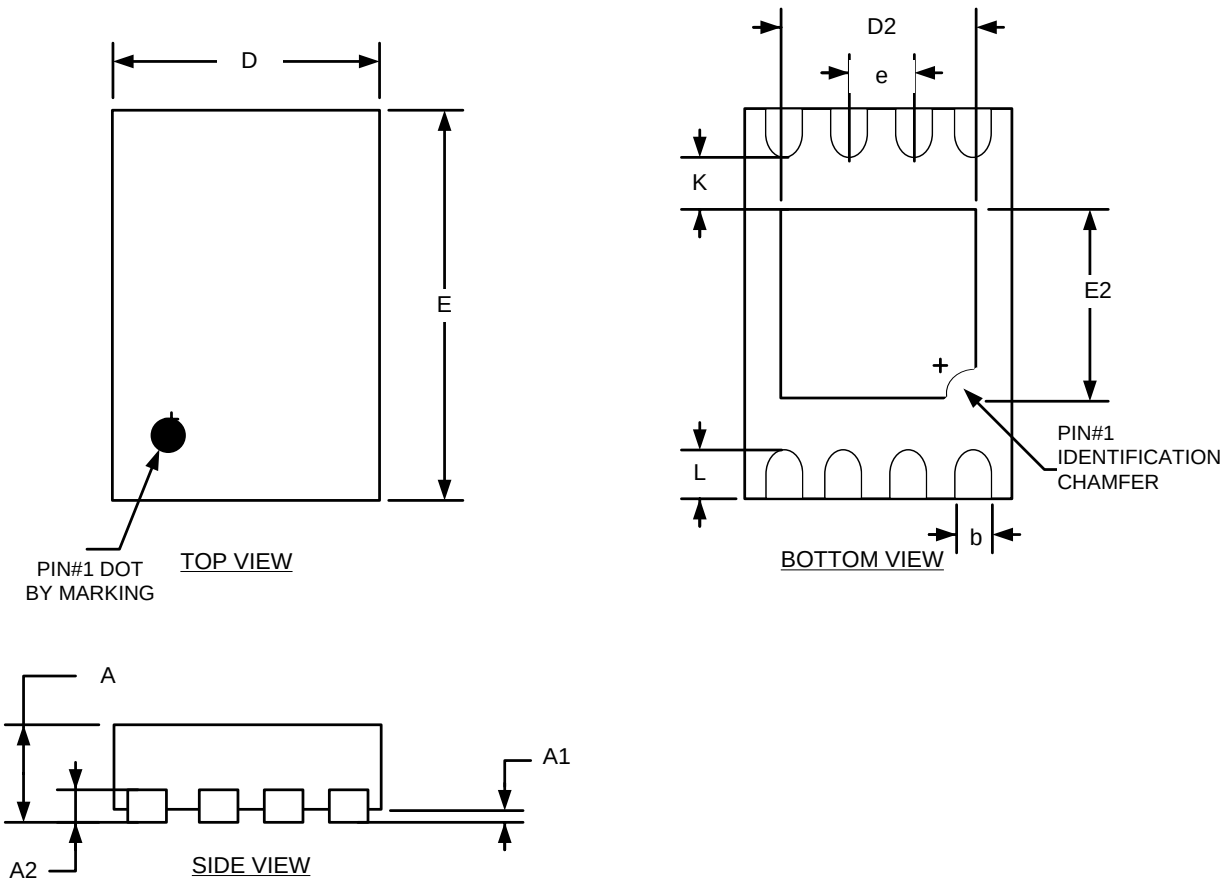


Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.230
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

10.3 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

11. Revision History

Revision	Date	Descriptions
V1.0	Oct. 2020	Initial version
V2.0	Apr. 2024	Update Trise